REMARKS

Claim 21 is amended. New claims 32-41 are added. No new matter is added as the originally-filed application supports the subject matter of the new claims at, for example, pages 8-10 and Figs. 5-6. Claims 21, 22 and 29-41 are pending in the application.

Claims 21 and 29-31 stand rejected under 35 U.S.C. §102(b) as being anticipated by Chen et al. (US Patent No. 5,472,896). Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Chen et al. (US Patent No. 5,472,896) in view of Ilg et al. (US Patent No. 6,130,145).

Claim 21 is amended. No new matter is added as the originally-filed application supports the amended language at, for example, Fig. 6. As amended, claim 21 recites a silicon-dioxide-containing dopant barrier layer against the metal-silicide layer, the metal-silicide layer comprising the only structure elevationally below and against the barrier layer. Chen teaches an thin oxide layer 22 formed over exposed surfaces of a gate electrode structure **and** a semiconductor substrate 10 (col. 4, lines 43-49) wherein the thin oxide layer 22 is **against** tungsten silicide layer 16 **and** semiconductor substrate 10. In no fair or reasonable interpretation does Chen teach or suggest a silicon-dioxide-containing dopant barrier layer against the metal-silicide layer wherein the metal-silicide layer comprises the only structure **elevationally below** and **against** the barrier layer as recited in claim 21. Accordingly, Chen fails to teach or suggest a positively recited limitation of claim 21.

Moreover, Ilg fails to teach or suggest a silicon-dioxide-containing dopant barrier layer against the metal-silicide layer, the metal-silicide layer comprising the only structure elevationally below and against the barrier layer as recited in claim 21. Consequently, it is inconceivable that Chen and Ilg, singularly or in any combination, could suggest or teach such positively recited limitation of claim 21, and therefore, an obviousness rejection based on the art of record would be inappropriate. Claim 21 is allowable and Applicant respectfully requests allowance of claim 21 in the next office action.

Claims 22 and 29-31 depend from independent claim 35, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are neither shown or taught by the art of record.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 7-8-02

By: 

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Application Serial No. 09/875,501
Filing Date ..... June 4, 2001
Inventor ..... Klaus Florian Schuegraf
Assignee ..... Micron Technology, Inc.
Group Art Unit 2815
Examiner ..... Edgardo Ortiz
Attorney's Docket No. MI22-1741
Title: Methods For Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 8, 2002 FINAL OFFICE ACTION TO ACCOMPANY RCE FILING

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

21. (Amended) A conductive line comprising:

a polysilicon layer;

a metal-silicide layer against the layer of polysilicon, the metal-silicide layer comprising a Group III dopant or a Group V dopant; and

a silicon-dioxide-containing dopant barrier layer against the metal-silicide layer, the metal-silicide layer comprising the only structure directly below and against the barrier layer.

Please add the following new claims:

32. (New) A conductive line comprising:

a polysilicon layer;

a doped metal-silicide layer against the polysilicon layer;

a silicon-dioxide-containing dopant barrier layer against the metal-silicide layer; and

the polysilicon layer, metal-silicide layer and barrier layer having aligned respective sidewalls, the aligned respective sidewalls defining an entirety of a lateral width for the conductive line.

33. (New) The conductive line of claim 32 wherein the doped metal-silicide layer comprises a Group III dopant or a Group V dopant.

34. (New) The conductive line of claim 32 wherein the silicon-dioxide-containing dopant barrier layer is against only the metal-silicide layer.

35. (New) The conductive line of claim 32 wherein the metal-silicide layer is doped to a concentration of at least about 1×10^{18} ions/cm^3.

36. (New) A conductive line comprising:

a polysilicon layer supported by a substrate;

a doped metal-silicide layer supported by the polysilicon layer; and

a silicon-dioxide-containing dopant barrier layer elevationally over the metal-silicide layer and substrate, and the barrier layer against only the metal-silicide layer with respect to the substrate and the metal-silicide layer.

37. (New) The conductive line of claim 36 wherein the doped metal-silicide layer comprises a Group III dopant or a Group V dopant.

38. (New) The conductive line of claim 36 wherein the polysilicon layer comprises a lateral width substantially equal to a lateral width of the conductive line.

39. (New) The conductive line of claim 36 wherein the metal-silicide layer is doped to a concentration of at least about 1×10^{18} ions/cm^3.

40. (New) The conductive line of claim 36 wherein the metal-silicide layer comprises a lateral width substantially equal to a lateral width of the conductive line.

41. (New) The conductive line of claim 36 wherein the silicon-dioxide-containing dopant barrier layer comprises a lateral width substantially equal to a lateral width of the conductive line.

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